

August 1996

NPN/PNP Transistor Arrays

Applications

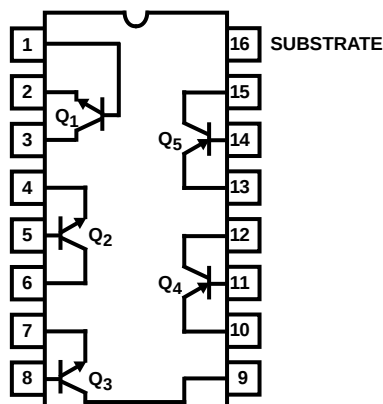
- Five-Independent Transistors
 - Three NPN and
 - Two PNP
- Differential Amplifiers
- DC Amplifiers
- Sense Amplifiers
- Level Shifters
- Timers
- Lamp and Relay Drivers
- Thyristor Firing Circuits
- Temperature Compensated Amplifiers
- Operational Amplifiers

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3096AE	-55 to 125	16 Ld PDIP	E16.3
CA3096AM (3096A)	-55 to 125	16 Ld SOIC	M16.15
CA3096AM96 (3096A)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3096CE	-55 to 125	16 Ld PDIP	E16.3
CA3096E	-55 to 125	16 Ld PDIP	E16.3
CA3096M (3096)	-55 to 125	16 Ld SOIC	M16.15
CA3096M96 (3096)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Pinout

CA3096, CA3096A, CA3096C
(PDIP, SOIC)
TOP VIEW



Description

The CA3096C, CA3096, and CA3096A are general purpose high voltage silicon transistor arrays. Each array consists of five independent transistors (two PNP and three NPN types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096A, CA3096, and CA3096C are identical, except that the CA3096A specifications include parameter matching and greater stringency in I_{CBO} , I_{CEO} , and $V_{CE(SAT)}$. The CA3096C is a relaxed version of the CA3096. To type this body text, simply triple click this paragraph and begin typing. The paragraph tag for this area is called body.

CA3096, CA3096A, CA3096C Essential Differences

CHARACTERISTIC	CA3096A	CA3096	CA3096C
$V_{(BR)CEO}$ (V) (Min)			
NPN	35	35	24
PNP	-40	-40	-24
$V_{(BR)CBO}$ (V) (Min)			
NPN	45	45	30
PNP	-40	-40	-24
h_{FE} at 1mA			
NPN	150-500	150-500	100-670
PNP	20-200	20-200	15-200
h_{FE} at 100μA			
PNP	40-250	40-250	30-300
I_{CBO} (nA) (Max)			
NPN	40	100	100
PNP	-40	-100	-100
I_{CEO} (nA) (Max)			
NPN	100	1000	1000
PNP	-100	-1000	-1000
$V_{CE SAT}$ (V) (Max)			
NPN	0.5	0.7	0.7
$ V_{IO} $ (mV) (Max)			
NPN	5	-	-
PNP	5	-	-
$ I_{IO} $ (μA) (Max)			
NPN	0.6	-	-
PNP	0.25	-	-

CA3096, CA3096A, CA3096C

Absolute Maximum Ratings

	NPN	PNP
Collector-to-Emitter Voltage, V_{CEO}		
CA3096, CA3096A	35V	-40V
CA3096C	24V	-24V
Collector-to-Base Voltage, V_{CBO}		
CA3096, CA3096A	45V	-40V
CA3096C	30V	-24V
Collector-to-Substrate Voltage, V_{CIO} (Note 1)		
CA3096, CA3096A	45V	-
CA3096C	30V	-
Emitter-to-Substrate Voltage, V_{EIO}		
CA3096, CA3096A	-	-40V
CA3096C	-	-24V
Emitter-to-Base Voltage, V_{EBO}		
CA3096, CA3096A	6V	-40V
CA3096C	6V	-24V
Collector Current, I_C (All Types)	50mA	-10mA

Operating Conditions

Temperature Range -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	170
Maximum Power Dissipation (Each Transistor, Note 3)	200mW
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3096 is isolated from the substrate by an integral diode. The substrate (Terminal 16) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. Care must be taken to avoid exceeding the maximum junction temperature. Use the total power dissipation (all transistors) and thermal resistances to calculate the junction temperature.

Electrical Specifications For Equipment Design, At $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	CA3096			CA3096A			CA3096C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS FOR EACH NPN TRANSISTOR											
I _{CBO}	V _{CB} = 10V, I _E = 0	-	0.001	100	-	0.001	40	-	0.001	100	nA
I _{CEO}	V _{CE} = 10V, I _B = 0	-	0.006	1000	-	0.006	100	-	0.006	1000	nA
V _{(BR)CEO}	I _C = 1mA, I _B = 0	35	50	-	35	50	-	24	35	-	V
V _{(BR)CBO}	I _C = 10μA, I _E = 0	45	100	-	45	100	-	30	80	-	V
V _{(BR)CIO}	I _{CI} = 10μA, I _B = I _E = 0	45	100	-	45	100	-	30	80	-	V
V _{(BR)EBO}	I _E = 10μA, I _C = 0	6	8	-	6	8	-	6	8	-	V
V _Z	I _Z = 10μA	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
V _{CE SAT}	I _C = 10mA, I _B = 1mA	-	0.24	0.7	-	0.24	0.5	-	0.24	0.7	V
V _{BE} (Note 4)	I _C = 1mA, V _{CE} = 5V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h _{FE} (Note 4)		150	390	500	150	390	500	100	390	670	
ΔV _{BE} /ΔT (Note 4)	I _C = 1mA, V _{CE} = 5V	-	1.9	-	-	1.9	-	-	1.9	-	mV/°C
DC CHARACTERISTICS FOR EACH PNP TRANSISTOR											
I _{CBO}	V _{CB} = -10V, I _E = 0	-	-0.06	-100	-	-0.006	-40	-	-0.06	-100	nA

CA3096, CA3096A, CA3096C

Electrical Specifications For Equipment Design, At $T_A = 25^\circ\text{C}$ (Continued)

PARAMETER	TEST CONDITIONS	CA3096			CA3096A			CA3096C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEO}	$V_{CE} = -10\text{V}$, $I_B = 0$	-	-0.12	-1000	-	-0.12	-100	-	-0.12	-1000	nA
$V_{(BR)CEO}$	$I_C = -100\mu\text{A}$, $I_B = 0$	-40	-75	-	-40	-75	-	-24	-30	-	V
$V_{(BR)CBO}$	$I_C = -10\mu\text{A}$, $I_E = 0$	-40	-80	-	-40	-80	-	-24	-60	-	V
$V_{(BR)EBO}$	$I_E = -10\mu\text{A}$, $I_C = 0$	-40	-100	-	-40	-100	-	-24	-80	-	V
$V_{(BR)EIO}$	$I_{EI} = 10\mu\text{A}$, $I_B = I_C = 0$	40	100	-	40	100	-	24	80	-	V
$V_{CE SAT}$	$I_C = -1\text{mA}$, $I_B = -100\mu\text{A}$	-	-0.16	-0.4	-	-0.16	-0.4	-	-0.16	-0.4	V
V_{BE} (Note 4)	$I_C = -100\mu\text{A}$, $V_{CE} = -5\text{V}$	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	V
h_{FE} (Note 4)	$I_C = -100\mu\text{A}$, $V_{CE} = -5\text{V}$	40	85	250	40	85	250	30	85	300	
	$I_C = -1\text{mA}$, $V_{CE} = -5\text{V}$	20	47	200	20	47	200	15	47	200	
$ \Delta V_{BE}/\Delta T $ (Note 4)	$I_C = -100\mu\text{A}$, $V_{CE} = -5\text{V}$	-	2.2	-	-	2.2	-	-	2.2	-	mV/ $^\circ\text{C}$

I_{CBO} Collector-Cutoff Current

V_Z Emitter-to-Base Zener Voltage

I_{CEO} Collector-Cutoff Current

$V_{CE SAT}$ Collector-to-Emitter Saturation Voltage

$V_{(BR)CEO}$ Collector-to-Emitter Breakdown Voltage

V_{BE} Base-to-Emitter Voltage

$V_{(BR)CBO}$ Collector-to-Base Breakdown Voltage

h_{FE} DC Forward-Current Transfer Ratio

$V_{(BR)CIO}$ Collector-to-Substrate Breakdown Voltage

$|\Delta V_{BE}/\Delta T|$ Magnitude of Temperature Coefficient:
(for each transistor)

$V_{(BR)EBO}$ Emitter-to-Base Breakdown Voltage

NOTE:

4. Actual forcing current is via the emitter for this test.

Electrical Specifications For Equipment Design At $T_A = 25^\circ\text{C}$ (CA3096A Only)

PARAMETER	SYMBOL	TEST CONDITIONS	CA3096A			UNITS
			MIN	TYP	MAX	
FOR TRANSISTORS Q ₁ AND Q ₂ (AS A DIFFERENTIAL AMPLIFIER)						
Absolute Input Offset Voltage	V _{IO}	V _{CE} = 5V, I _C = 1mA	-	0.3	5	mV
Absolute Input Offset Current	I _{IO}		-	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient	$\frac{ \Delta V_{IO} }{\Delta T}$		-	1.1	-	μV/°C
FOR TRANSISTORS Q ₄ AND Q ₅ (AS A DIFFERENTIAL AMPLIFIER)						
Absolute Input Offset Voltage	V _{IO}	V _{CE} = -5V, I _C = -100μA R _S = 0	-	0.15	5	mV
Absolute Input Offset Current	I _{IO}		-	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient	$\frac{ \Delta V_{IO} }{\Delta T}$		-	0.54	-	μV/°C

CA3096, CA3096A, CA3096C

Electrical Specifications

Typical Values Intended Only for Design Guidance At $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
DYNAMIC CHARACTERISTICS FOR EACH NPN TRANSISTOR				
Noise Figure (Low Frequency)	NF	$f = 1\text{kHz}$, $V_{CE} = 5\text{V}$, $I_C = 1\text{mA}$, $R_S = 1\text{k}\Omega$	2.2	dB
Low-Frequency, Input Resistance	R_I	$f = 1.0\text{kHz}$, $V_{CE} = 5\text{V}$, $I_C = 1\text{mA}$	10	$\text{k}\Omega$
Low-Frequency Output Resistance	R_O	$f = 1.0\text{kHz}$, $V_{CE} = 5\text{V}$, $I_C = 1\text{mA}$	80	$\text{k}\Omega$
Admittance Characteristics				
Forward Transfer Admittance	y_{FE}	g_{FE} $f = 1\text{MHz}$, $V_{CE} = 5\text{V}$, $I_C = 1\text{mA}$	7.5	mS
		b_{FE} $f = 1\text{MHz}$, $V_{CE} = 5\text{V}$, $I_C = 1\text{mA}$	-j13	mS
Input Admittance	y_{IE}	g_{IE} $f = 1\text{MHz}$, $V_{CE} = 5\text{V}$, $I_C = 1\text{mA}$	2.2	mS
		b_{IE} $f = 1\text{MHz}$, $V_{CE} = 5\text{V}$, $I_C = 1\text{mA}$	j3.1	mS
Output Admittance	y_{OE}	g_{OE} $f = 1\text{MHz}$, $V_{CE} = 5\text{V}$, $I_C = 1\text{mA}$	0.76	mS
		b_{OE} $f = 1\text{MHz}$, $V_{CE} = 5\text{V}$, $I_C = 1\text{mA}$	j2.4	mS
Gain-Bandwidth Product	f_T	$V_{CE} = 5\text{V}$, $I_C = 1.0\text{mA}$	280	MHz
		$V_{CE} = 5\text{V}$, $I_C = 5\text{mA}$	335	MHz
Emitter-To-Base Capacitance	C_{EB}	$V_{EB} = 3\text{V}$	0.75	pF
Collector-To-Base Capacitance	C_{CB}	$V_{CB} = 3\text{V}$	0.46	pF
Collector-To-Substrate Capacitance	C_{CI}	$V_{CI} = 3\text{V}$	3.2	pF
DYNAMIC CHARACTERISTICS FOR EACH PNP TRANSISTOR				
Noise Figure (Low Frequency)	NF	$f = 1\text{kHz}$, $I_C = 100\mu\text{A}$, $R_S = 1\text{k}\Omega$	3	dB
Low-Frequency Input Resistance	R_I	$f = 1\text{kHz}$, $V_{CE} = 5\text{V}$, $I_C = 100\mu\text{A}$	27	$\text{k}\Omega$
Low-Frequency Output Resistance	R_O	$f = 1\text{kHz}$, $V_{CE} = 5\text{V}$, $I_C = 100\mu\text{A}$	680	$\text{k}\Omega$
Gain-Bandwidth Product	f_T	$V_{CE} = 5\text{V}$, $I_C = 100\mu\text{A}$	6.8	MHz
Emitter-To-Base Capacitance	C_{EB}	$V_{EB} = -3\text{V}$	0.85	pF
Collector-To-Base Capacitance	C_{CB}	$V_{CB} = -3\text{V}$	2.25	pF
Base-To-Substrate Capacitance	C_{BI}	$V_{BI} = 3\text{V}$	3.05	pF

Typical Applications

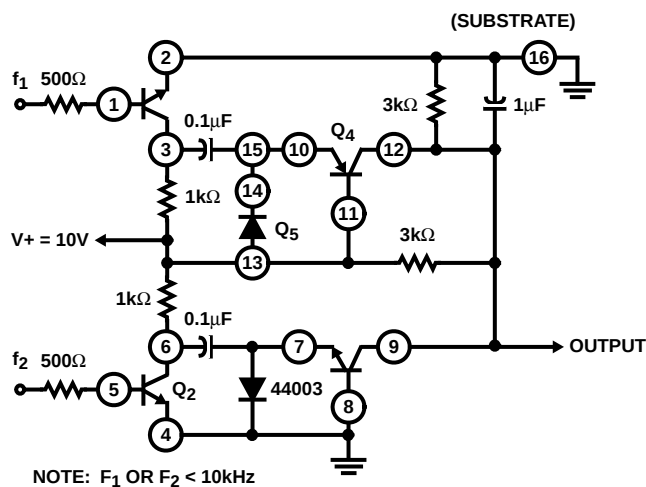


FIGURE 1. FREQUENCY COMPARATOR USING CA3096

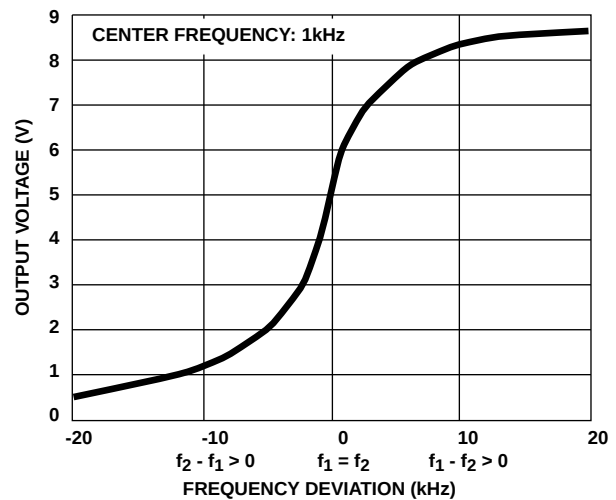


FIGURE 2. FREQUENCY COMPARATOR CHARACTERISTICS

Typical Applications (Continued)

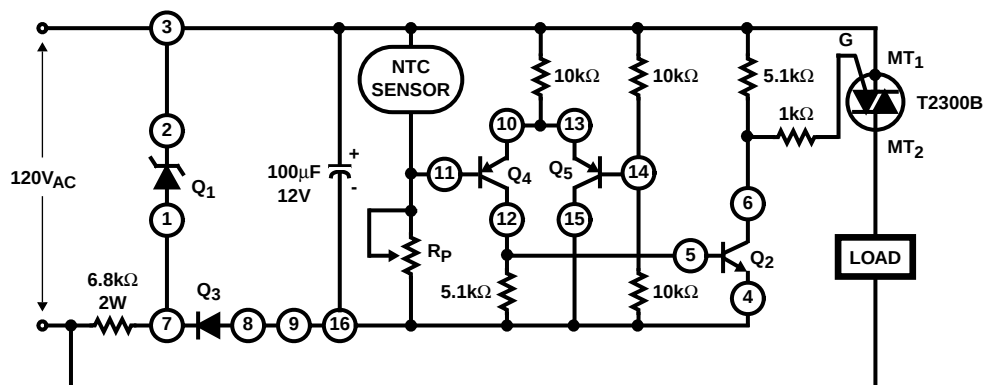
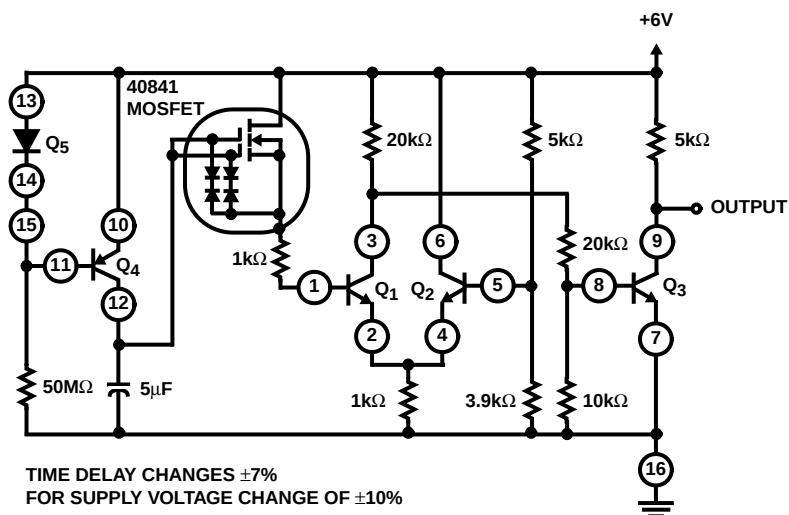


FIGURE 3. LINE-OPERATED LEVEL SWITCH USING CA3096A OR CA3096



TIME DELAY CHANGES $\pm 7\%$
FOR SUPPLY VOLTAGE CHANGE OF $\pm 10\%$

FIGURE 4. ONE-MINUTE TIMER USING CA3096A AND A MOSFET

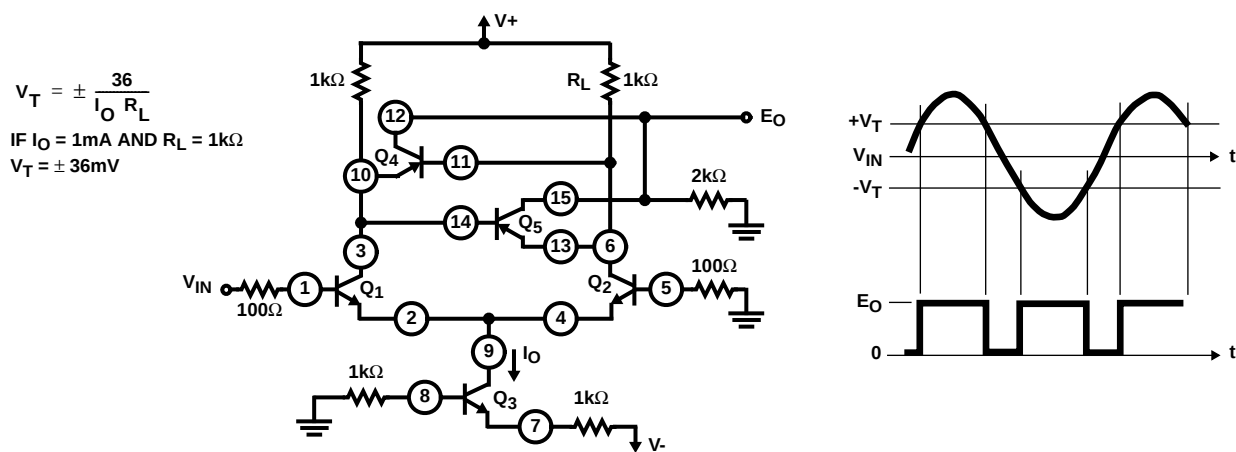


FIGURE 5. CA3096A SMALL-SIGNAL ZERO VOLTAGE DETECTOR HAVING NOISE IMMUNITY

Typical Applications (Continued)

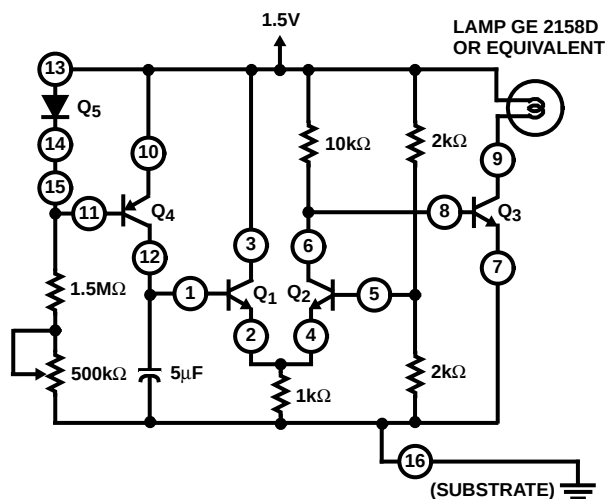
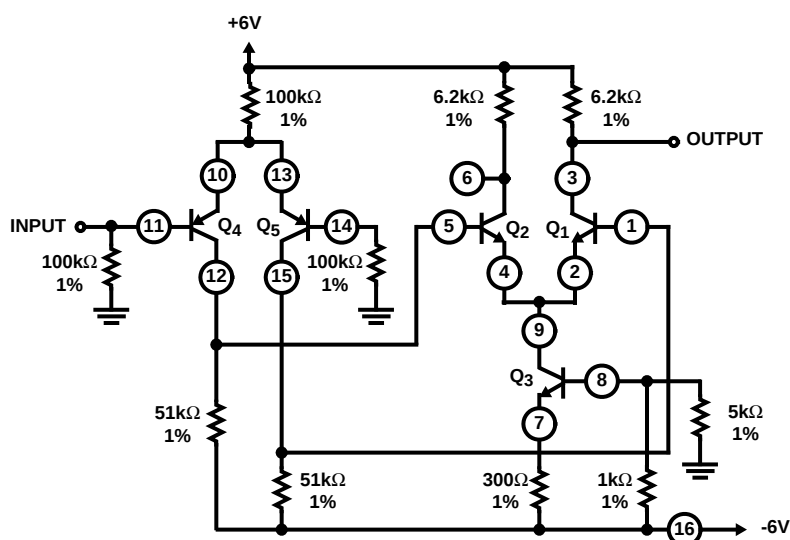


FIGURE 6. TEN-SECOND TIMER OPERATED FROM 1.5V SUPPLY USING CA3096



NOTES:

5. Can be operated with either dual supply or single supply.
6. Wide-input common mode range +5V to -5V.
7. Low bias current: <1μA.

FIGURE 7. CASCADE OF DIFFERENTIAL AMPLIFIERS USING CA3096A

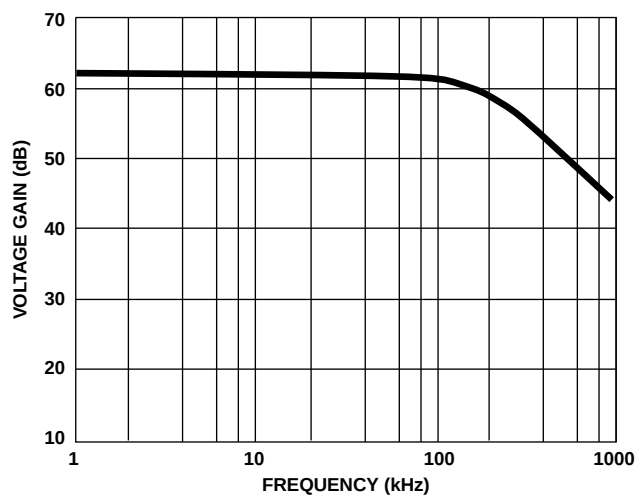


FIGURE 8. FREQUENCY RESPONSE

Typical Performance Curves

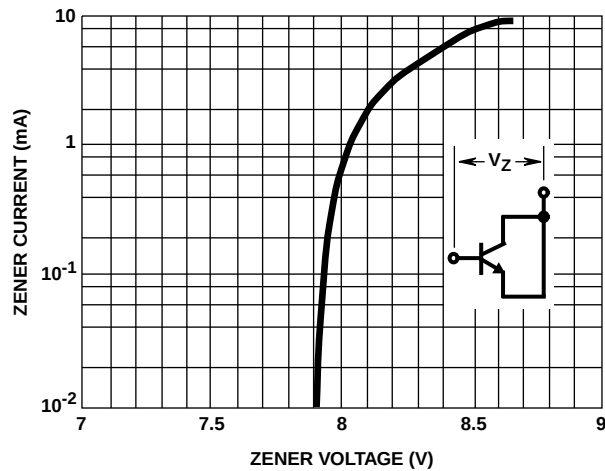


FIGURE 9. BASE-TO-EMITTER ZENER CHARACTERISTIC (NPN)

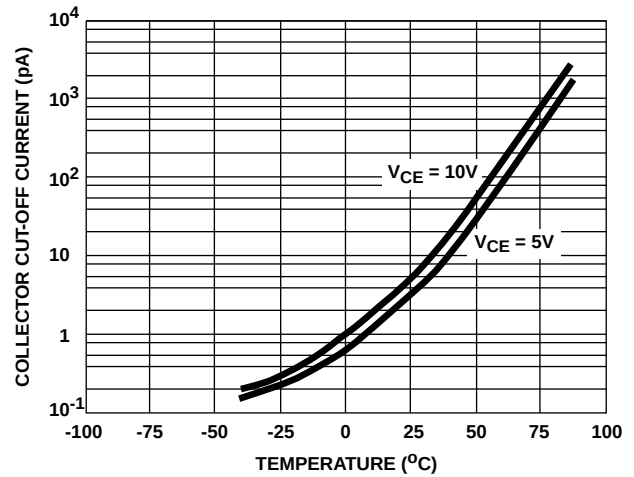


FIGURE 10. COLLECTOR CUT-OFF CURRENT (I_{CEO}) vs TEMPERATURE (NPN)

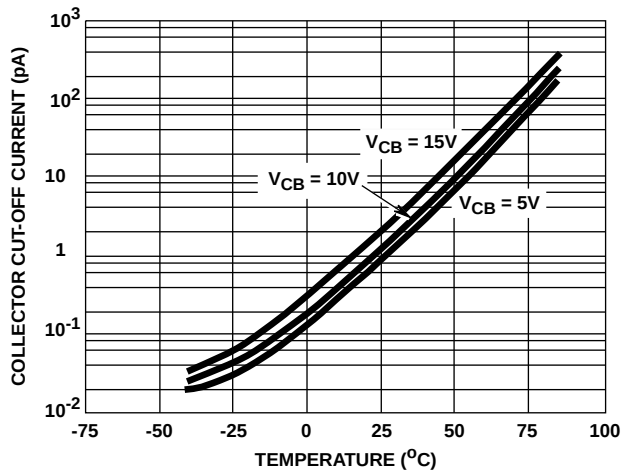


FIGURE 11. COLLECTOR CUT-OFF CURRENT (I_{CBO}) vs TEMPERATURE (NPN)

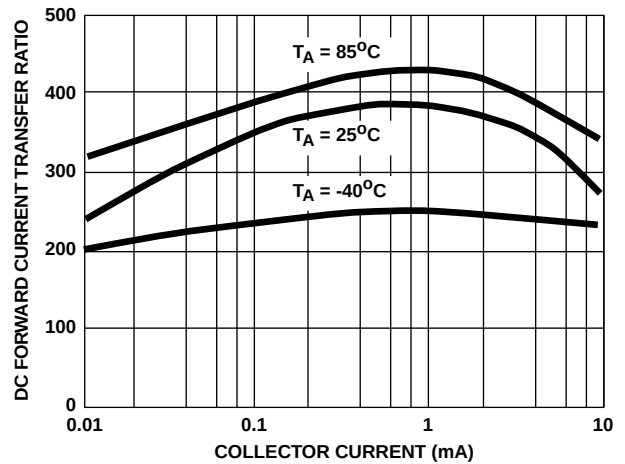


FIGURE 12. TRANSISTOR (NPN) h_{FE} vs COLLECTOR CURRENT

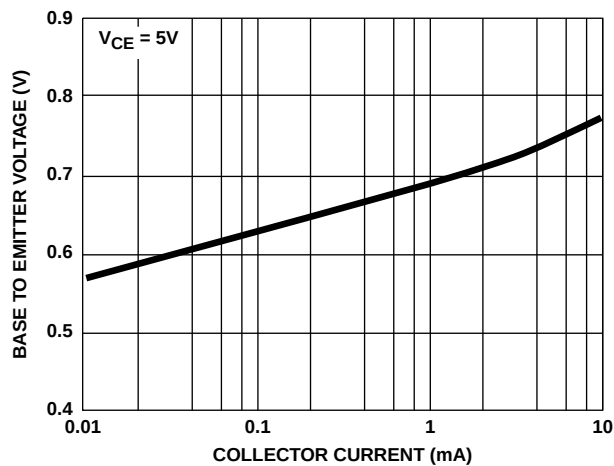


FIGURE 13. V_{BE} (NPN) vs COLLECTOR CURRENT

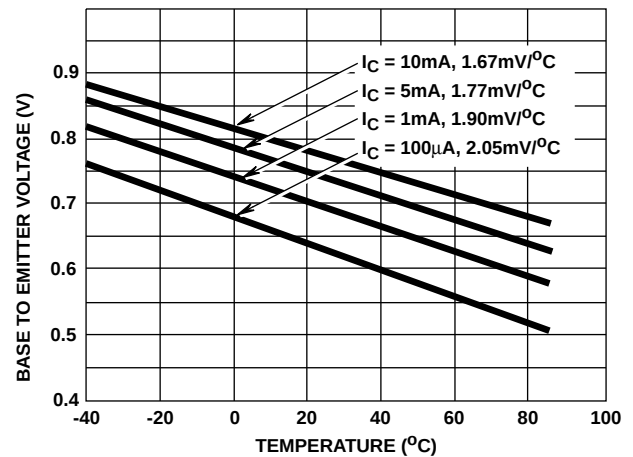


FIGURE 14. V_{BE} (NPN) vs TEMPERATURE

Typical Performance Curves (Continued)

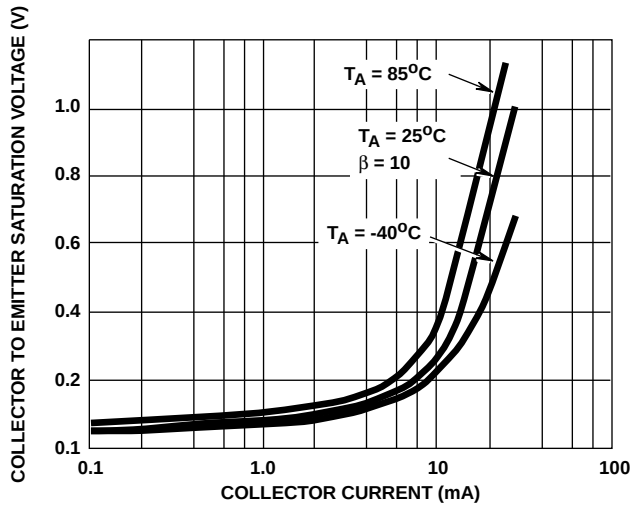


FIGURE 15. $V_{CE\text{ SAT}}$ (NPN) vs COLLECTOR CURRENT

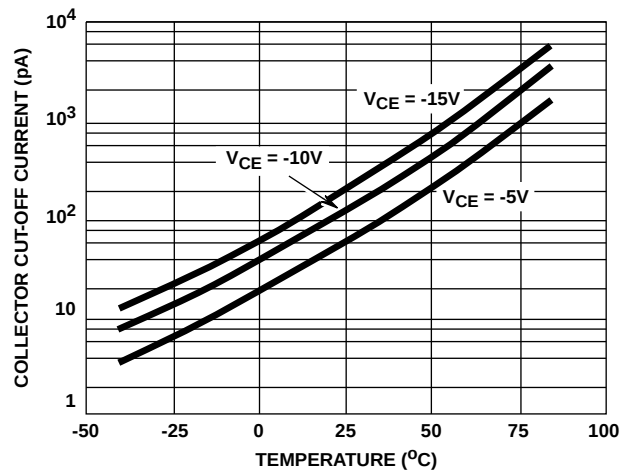


FIGURE 16. COLLECTOR CUT-OFF CURRENT (I_{CEO}) vs TEMPERATURE (PNP)

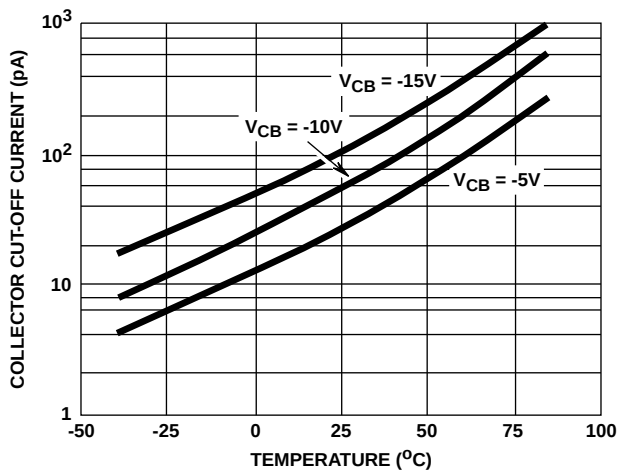


FIGURE 17. COLLECTOR CUT-OFF CURRENT (I_{CBO}) vs TEMPERATURE (PNP)

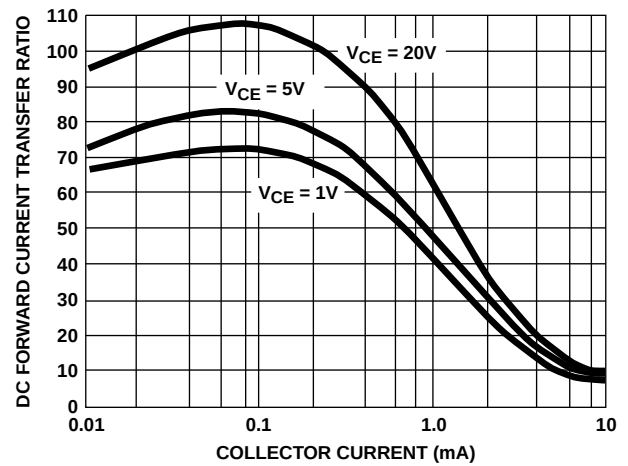


FIGURE 18. TRANSISTOR (PNP) h_{FE} vs COLLECTOR CURRENT

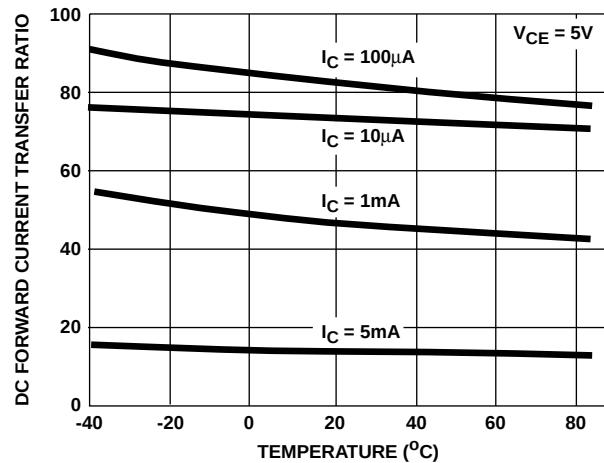


FIGURE 19. TRANSISTOR (PNP) h_{FE} vs TEMPERATURE

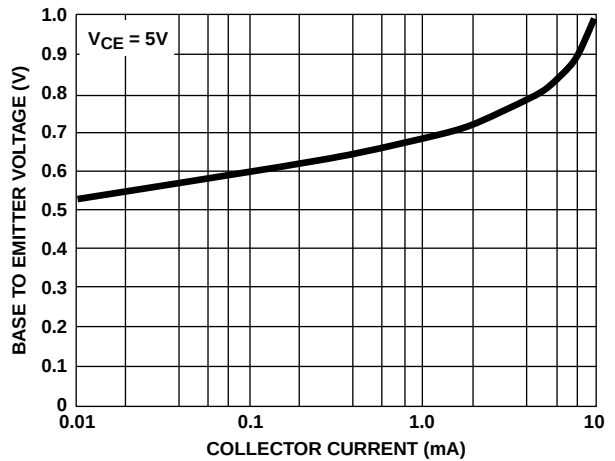


FIGURE 20. V_{BE} (PNP) vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

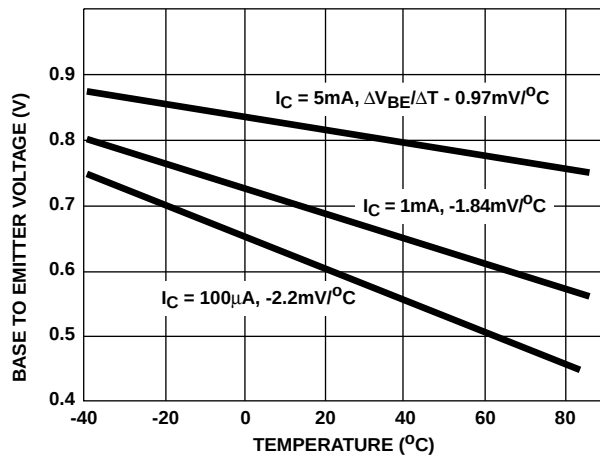


FIGURE 21. V_{BE} (PNP) vs TEMPERATURE

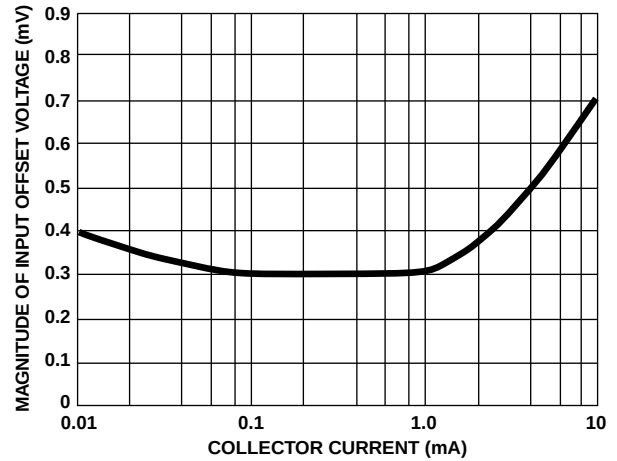


FIGURE 22. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR NPN TRANSISTOR $Q_1 - Q_2$

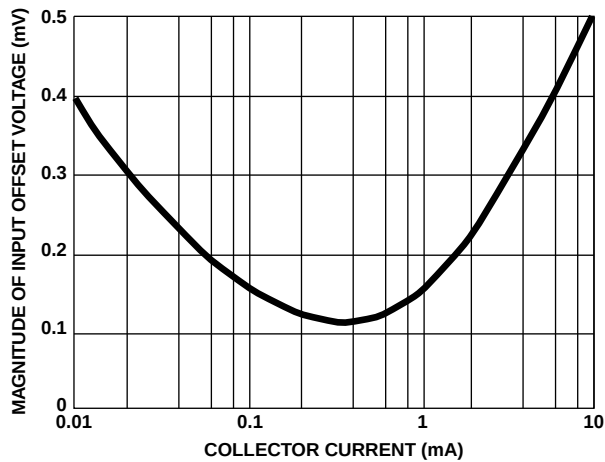


FIGURE 23. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR PNP TRANSISTOR $Q_4 - Q_5$

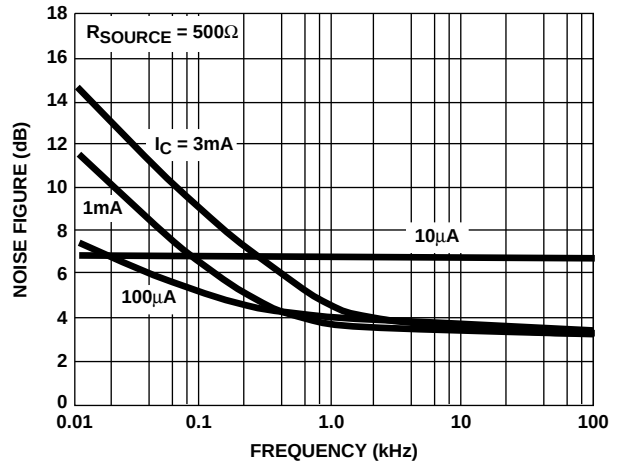


FIGURE 24. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

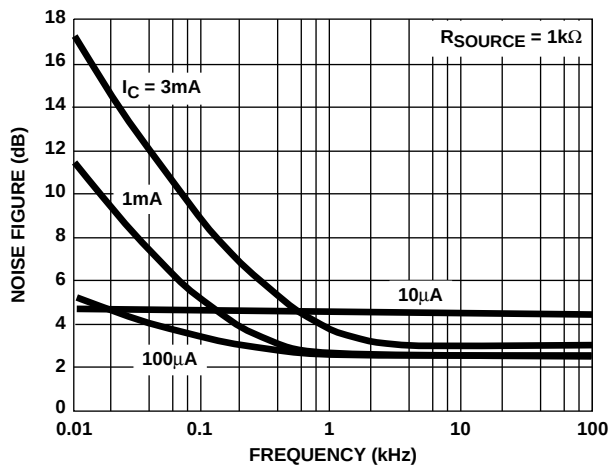


FIGURE 25. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

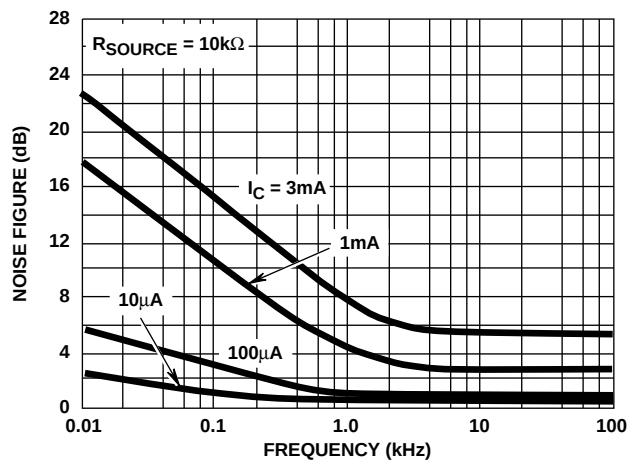


FIGURE 26. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

Typical Performance Curves (Continued)

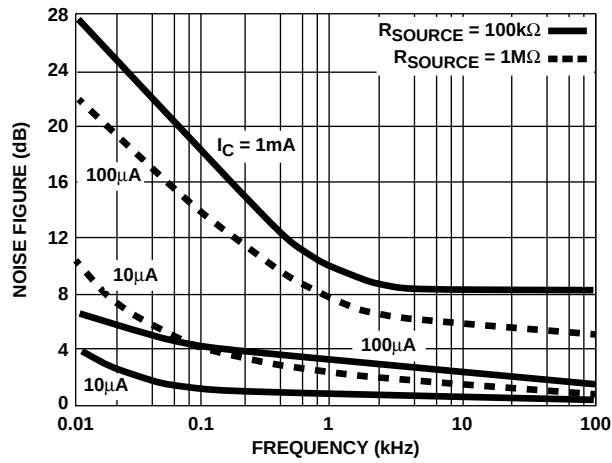


FIGURE 27. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

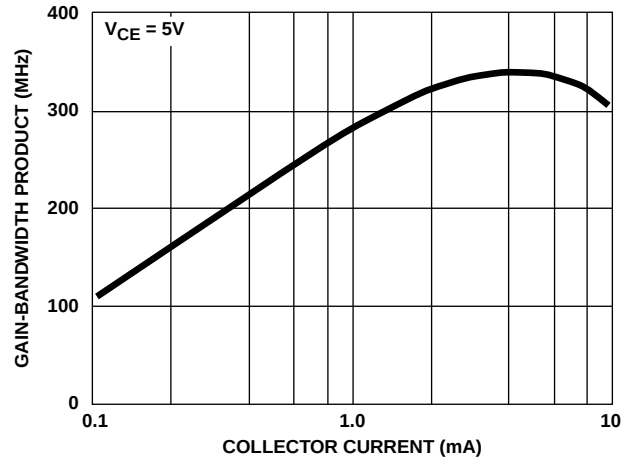


FIGURE 28. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (NPN)

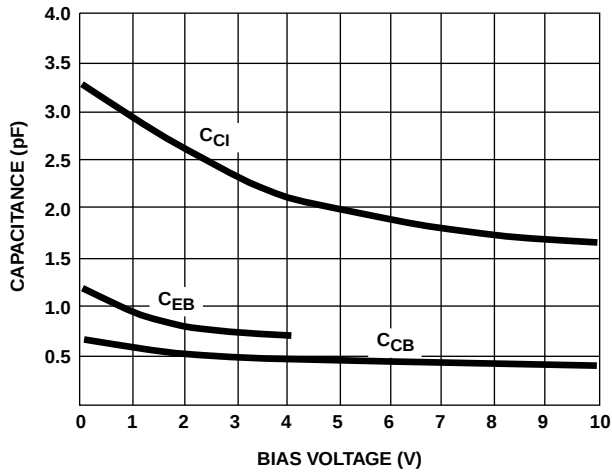


FIGURE 29. CAPACITANCE vs BIAS VOLTAGE (NPN)

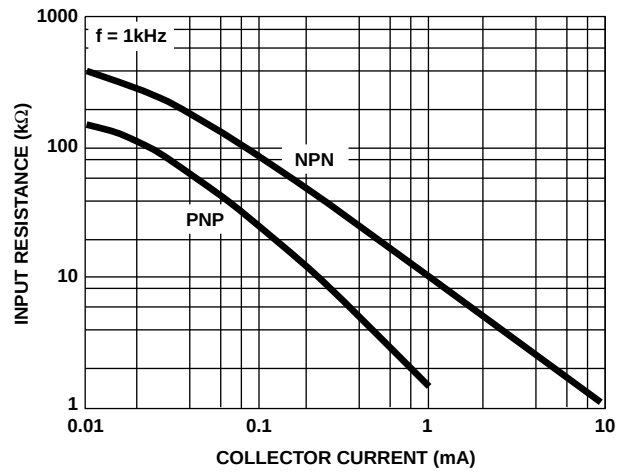


FIGURE 30. INPUT RESISTANCE vs COLLECTOR CURRENT

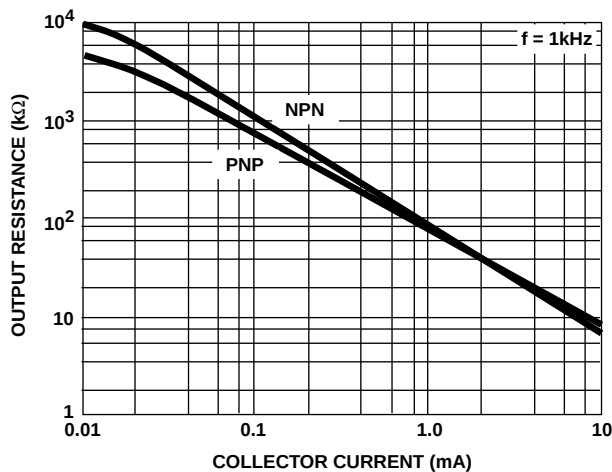


FIGURE 31. OUTPUT RESISTANCE vs COLLECTOR CURRENT

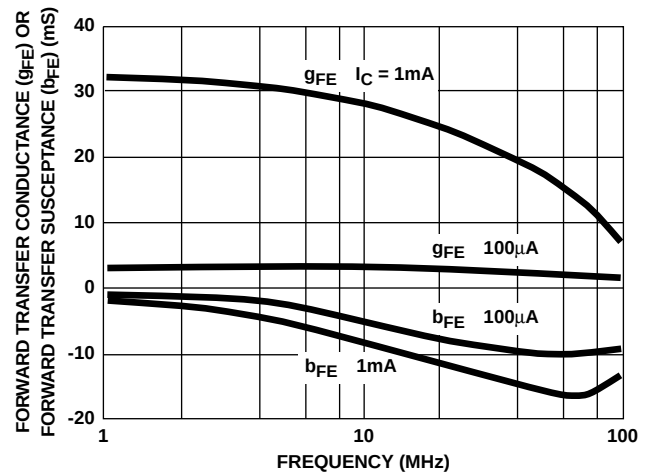


FIGURE 32. FORWARD TRANSCONDUCTANCE vs FREQUENCY

Typical Performance Curves (Continued)

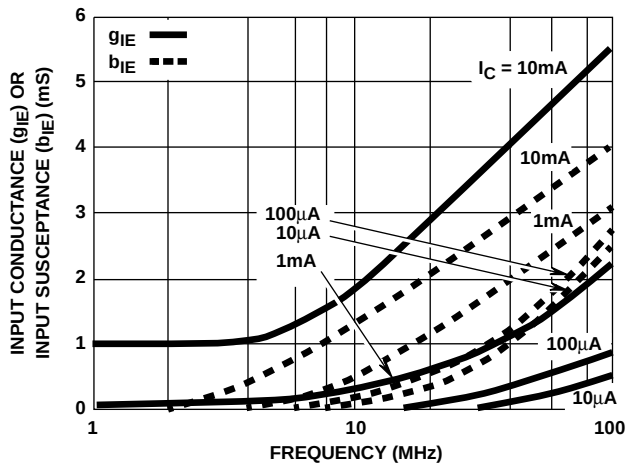


FIGURE 33. INPUT ADMITTANCE vs FREQUENCY

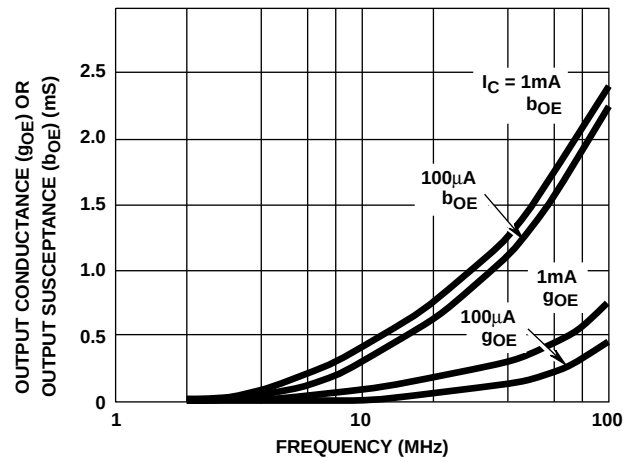


FIGURE 34. OUTPUT ADMITTANCE vs FREQUENCY

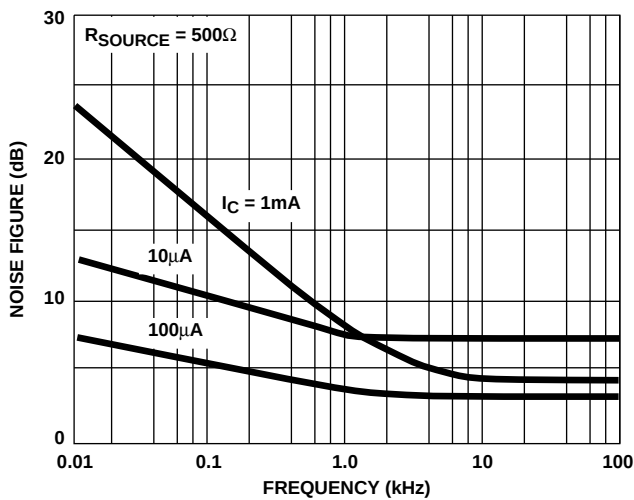


FIGURE 35. NOISE FIGURE vs FREQUENCY (PNP)

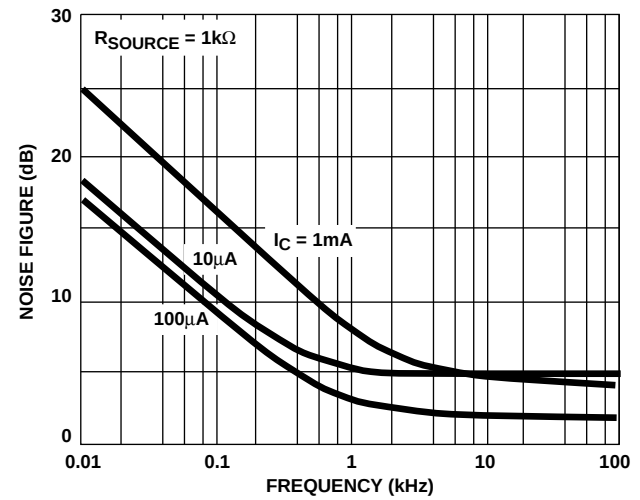


FIGURE 36. NOISE FIGURE vs FREQUENCY (PNP)

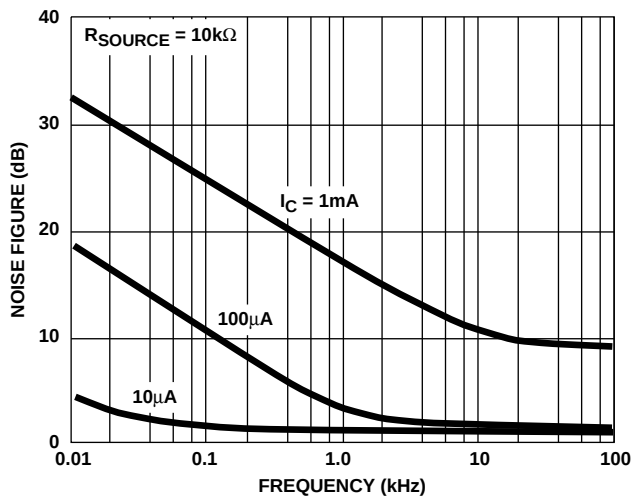


FIGURE 37. NOISE FIGURE vs FREQUENCY (PNP)

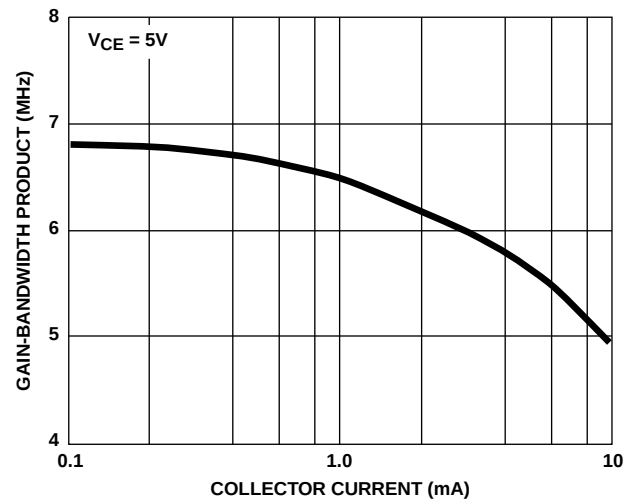


FIGURE 38. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (PNP)

Typical Performance Curves (Continued)

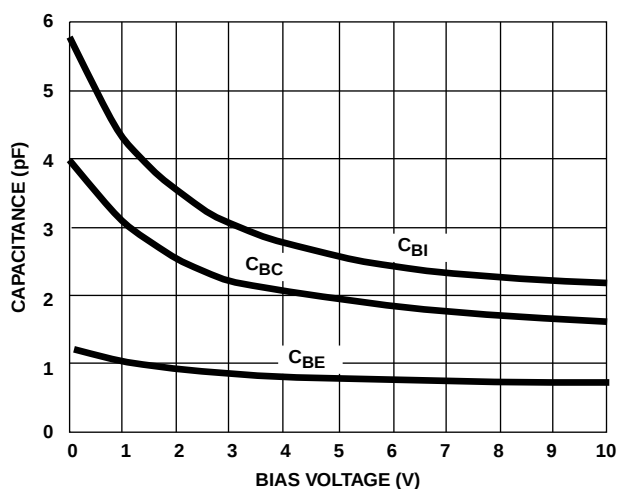
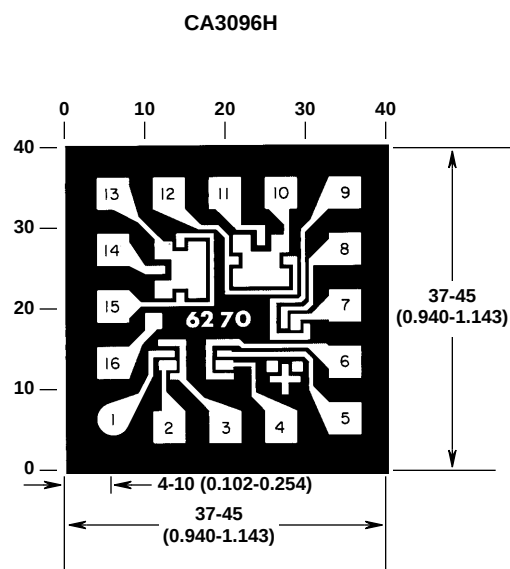


FIGURE 39. CAPACITANCE vs BIAS VOLTAGE (PNP)

Metallization Mask Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57 degrees instead of 90 degrees with respect to the face of the chip. Therefore, the isolated chip is actually 7mils (0.17mm) larger in both dimensions.